Mody University of Science and Technology

Lakshmangarh

Faculty of Engineering and Technology

Design of Operational Transconductance Amplifier and its Applications

Research Proposal

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Chapter – 1

OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

1.1 INTRODUCTION:

The evolution of very large scale integration (VLSI) technology has developed to the point where millions of transistors can be integrated on a single die or "chip". Integrated circuits once filled the role of subsystem components, partitioned at analog-digital boundaries; they now integrate complete system on a chip by combining both analog and digital functions. . With the quick improvements of computer aided design (CAD) tools, advancements of semiconductor modeling, steady miniaturization of transistor scaling, and the progress of fabrication processes, the integrated circuit market is growing rapidly. Nowadays, complementary metal-oxide semiconductor (CMOS) technology has become dominant over bipolar technology for analog circuit design in a mixed-signal system due to the industry trend of applying standard process technologies to implement both analog circuits and digital circuits on the same chip. Complementary Metal-oxide semiconductor (CMOS) technology has been the mainstay in mixed-signal implementations because it provides density and power savings on digital side, and a good mix of components for analog design. In a few years from now CMOS technology will overpower the whole electronic industry. While many digital circuits can be adapted to a smaller device level with a smaller power supply, most existing analog circuitry requires considerable change or even a redesign to accomplish the same feat. With transistor length being scaled down to a few tens of nanometers, analog circuits are becoming increasingly more difficult to improve upon. Designing high performance analog circuits is becoming increasingly challenging with the persistent trend toward reduced supply voltages. In an effort to increase the intrinsic gain of CMOS devices, the trend in the MOSFET design industry is to shrink the gate oxide thickness, t_{ox}, which unfortunately reduced the tolerance at the gate for high voltage levels. So, for reliability purposes, it is advantageous to reduce the maximum voltage V_{DD} but this trend of supply voltage reduction forces analog designers to face challenges such as reduced input common mode range, output swing and linearity. Designing of high performance analog circuits is becoming more challenging with the persistent trend towards reduced supply voltages as V_{TO}

does not scale in a linear fashion with the reduction in minimum device length at the same rate as V_{DD}.

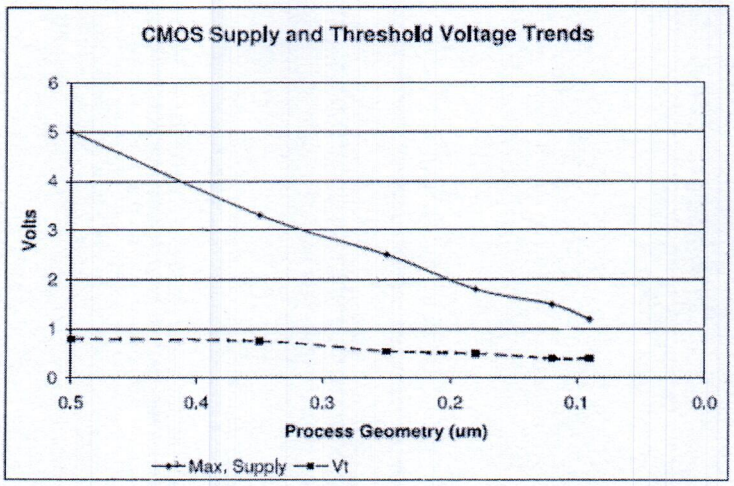


Figure (1) CMOS operating voltage trends in advanced silicon processes

The expressions for a short channel MOSFET transition frequency (f_T) and open loop gain ($g_m.r_0$) are given as [7] and [1]:

$$f_T \propto \frac{V_{OV}}{L}$$

$$g_m r_0 \propto \frac{L}{V_{OV}}$$

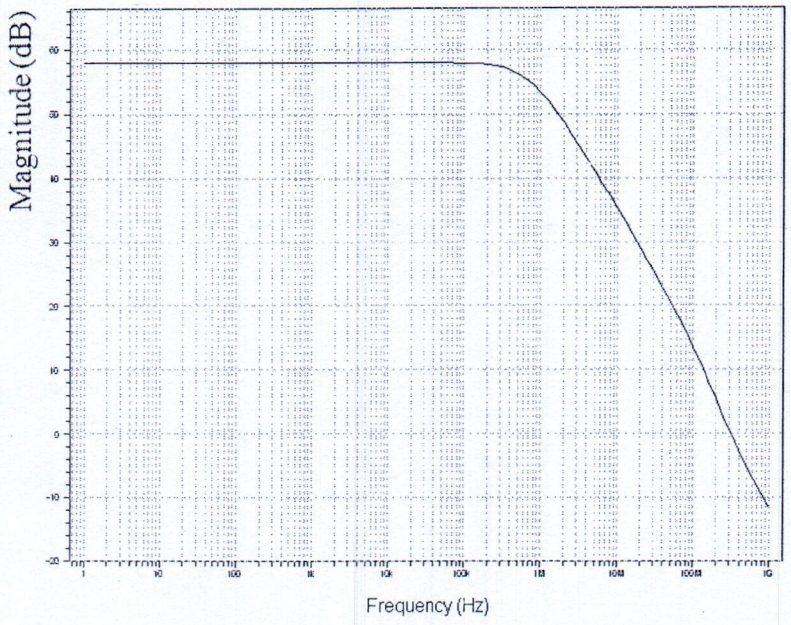
Where V_{ov}, L, g_m, and ro are the overdrive voltage, channel length, transconductance and output resistance respectively for a MOSFET. From these relations, it can be observed that downward scaling in gate length results in a larger f_T, and hence faster transistors. But higher speed comes at the cost of a reduction in transistor's open loop gain. Hence the amplifiers designed with scaled process exhibit larger bandwidths but lower open loop gains.

The main bottleneck in an analog circuit is Operational transconductance Amplifier. Operational transconductance Amplifiers (usually referred to as ota) have become one of the most versatile building blocks in analog processing system and are an integral part of many analog and mixed-signal systems. Operational transconductance Amplifiers are one of the indispensable blocks of modern integrated systems and are used in wide varieties of circuit topologies like data converters, filters, references, clock and data recovery circuits. However, continued scaling in CMOS processes has continuously challenged the established paradigms for operational transconductance amplifier (ota) design. Ota with vastly different levels of

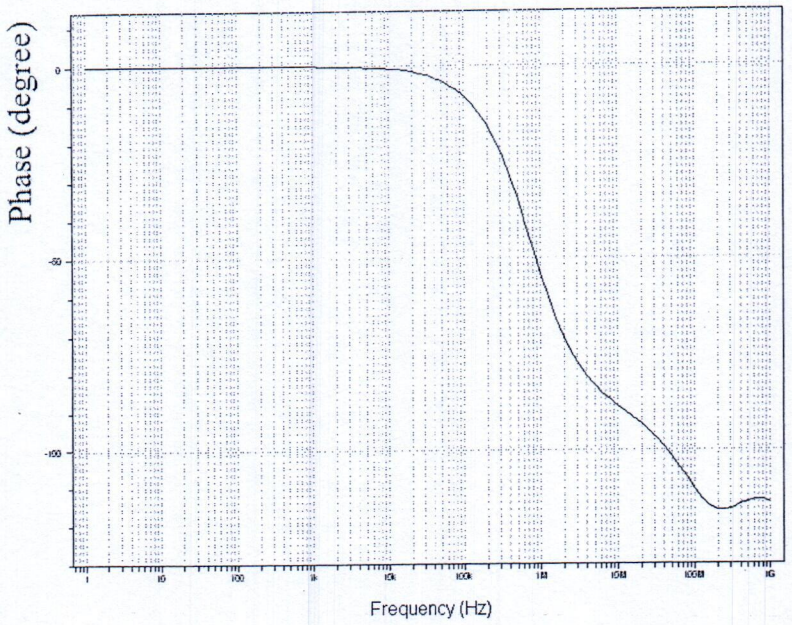
The circuit symbol of OTA is shown in Fig. 2. Ideally the OTA is assumed to be the voltage-controlled current source and is described mathematically as

$$I_o = g_m(V_1 - V_2) \tag{1}$$

Where I_0 is the output current, V_1 and V_2 denote the non-inverting and inverting input



(a)



(b)

Figure (4) Frequency response (a) Magnitude and (b) phase

voltages, respectively, of the OTA. Fig. 3 shows the CMOS implementation of the simple OTA [4]. Fig. 4 is showing the frequency response of the OTA. It uses only four MOS transistors and one current source. The M_1 and M_2 are perfectly matched transistors and the current mirrors are formed with M3 and M4 having unity current gain. Assuming all four MOS transistors operating in saturation region, the transconductance gain (g_m) of OTA can be expressed as

$$g_m = \sqrt{2\beta I_{abc}} \tag{2}$$

Note that β denotes the current factor [9]. It can be seen that β can be given by $\mu_n C_{ox}(W/L)_n$ and $\mu_p C_{ox}(W/L)_p$ for the NMOS differential pair based OTA and the corresponding PMOS respectively. Where μ is the mobility of the carrier, C_{ox} is the gate oxide capacitance per unit area, W is the effective channel width, L is the effective channel length. From Eq. (2), the g_m is proportional to $(I_{abc})^{1/2}$.

1.2 Commonly used topology for OTA:

There are several available OTA architectures. A few popular topologies, which broadly cover all the CMOS OTA, are discussed below:

1. Single Stage OTA
2. Two Stage OTA
3. Telescopic Cascode OTA
4. Regulated Cascode (Gain Boosting) OTA
5. Folded Cascode OTA

1. Single Stage OTA

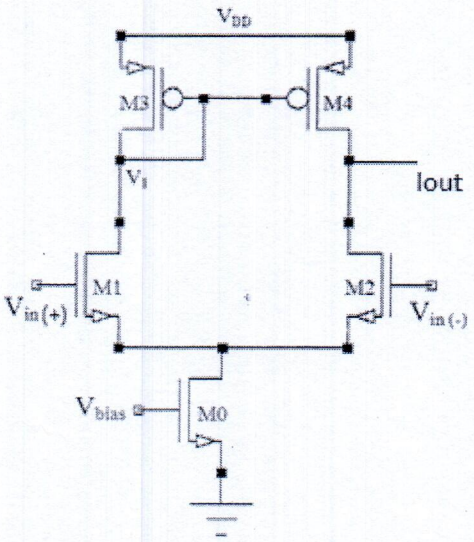


Figure (5) Single Stage OTA

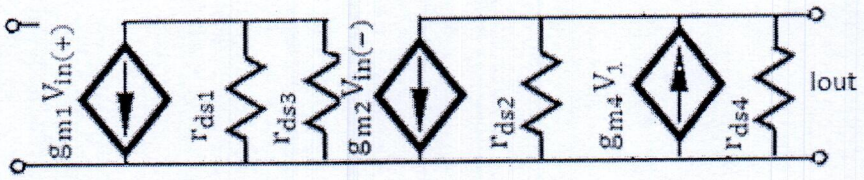


Figure (6) Small signal model of single stage OTA

Gain and output resistance is given as:

$$A_v(\text{Gain}) = -g_{m1}\left[\frac{1}{\frac{1}{r_{ds2}}+\frac{1}{r_{ds4}}}\right]$$

$$r_{out} = \frac{r_{ds2}r_{ds4}}{r_{ds2}+r_{ds4}}$$

The schematic of single stage op amp is shown in fig. 5. All the four transistors from M1-M4 contribute to input noise. The gain of such amplifier is limited and can not be used for practical applications. In order to achieve high gain other topologies can be used.

2. Two Stage OTA

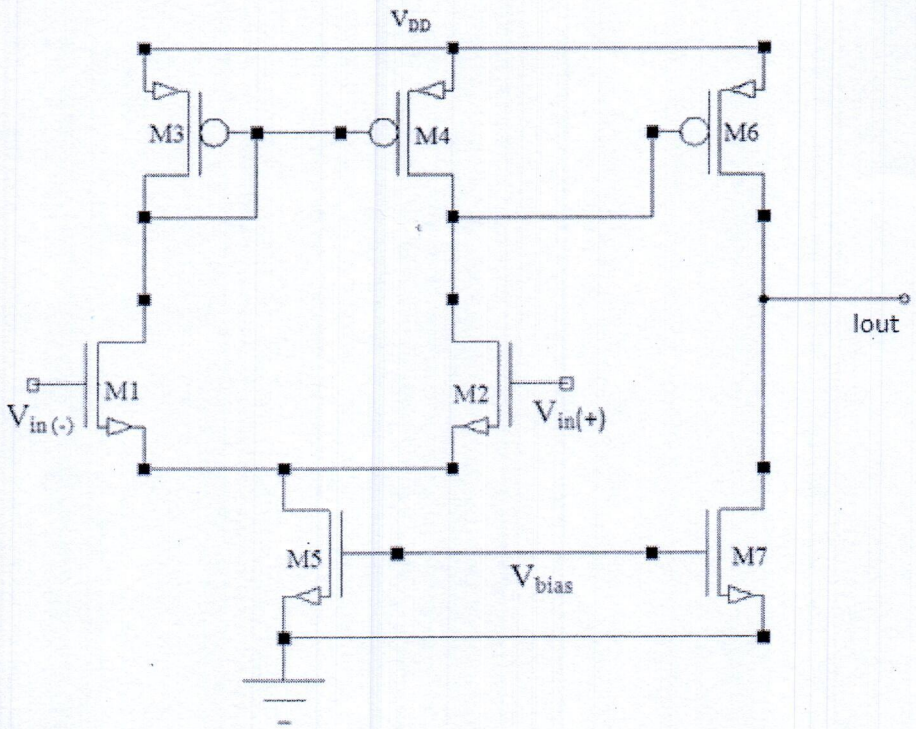


Figure (7) Two-stage OTA

Circuit Operation

The final circuit designed of two stage ota is shown in fig. 7. The topology of this circuit is that of a standard CMOS ota. It comprised of two subsections of circuits, namely differential gain stage, second gain stage. It was found that this topology was able to successfully meet all of the design specifications.

Differential Gain Stage

The first subsection of interest is the differential gain stage which is comprised of transistors M1 through M4. Transistors M1 and M2 are standard N channel MOSFET (NMOS) transistors which form the basic input stage of the amplifier. The gate of M1 is the inverting input and the gate of M2 is the non-inverting input. A differential input signal applied across the two input terminals will be amplified according to the gain of the differential stage. The gain of the stage is simply the transconductance of M2 times the total output resistance seen at the drain of M2. The two main resistances that contribute to the output resistance are that of the input transistors themselves and also the output resistance of the active load transistors, M3 and M4.

The current mirror active load used in this circuit has two distinct advantages.

1. The use of active load devices creates a large output resistance in a relatively small amount of die area.
2. The current mirror topology performs the differential to single-ended conversion of the input signal

Second Gain Stage

The purpose of the second gain stage, as the name implies, is to provide additional gain in the amplifier. Consisting of transistors M6 and M7, this stage takes the output from the drain of M2 and amplifies it through M6 which is in the standard common source configuration. Again, similar to the differential gain stage, this stage employs an active device, M7, to serve as the load resistance for M6. The gain of this stage is the transconductance of M6 times the effective load resistance comprised of the output resistances of M6 and M7.

A two-stage ota consists of a cascade of V→ I and I→ V stages as shown in fig. 8. The first stage consists of a differential amplifier converting the differential input voltage to differential currents. These differential currents are applied to a current mirror load recovering the differential voltage. The second stage consists of a common-source MOSFET converting the second stage input voltage to current. This transistor is loaded by a current-sink load, which converts the current to voltage at the output. The second stage is nothing more than a current-sink inverter.

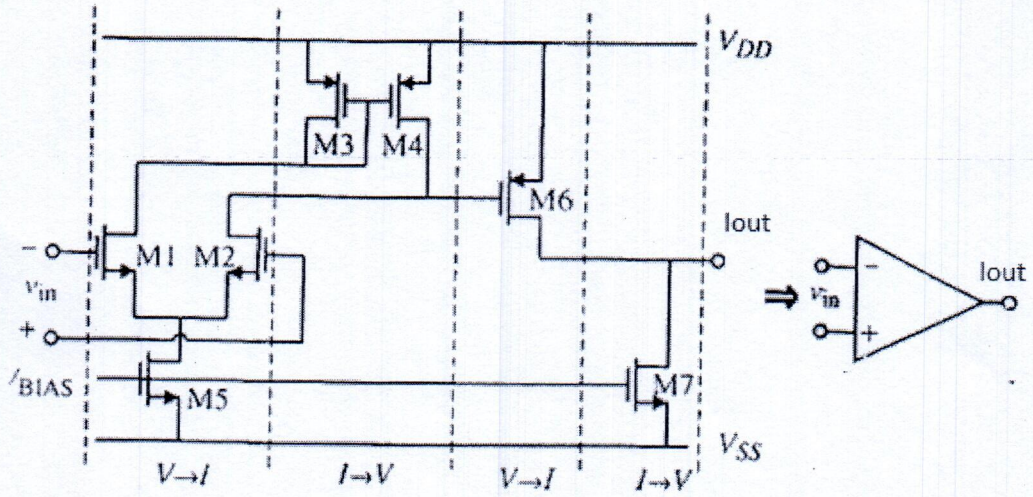


Figure (8) Two-stage OTA broken into V-I and I-V stages

Small Signal Model:

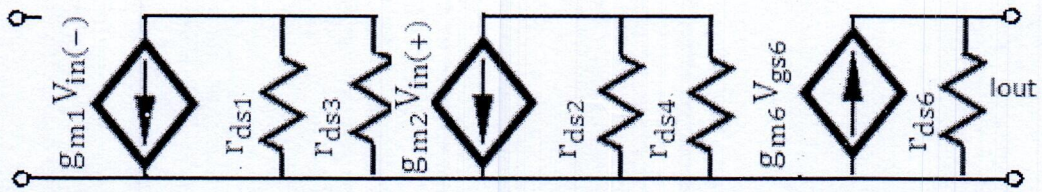


Figure (9) Small signal model of two stage OTA

Gain $A_v = -\frac{g_{m1} g_{m6} r_{ds6}}{\left(\frac{1}{r_{ds2}} + \frac{1}{r_{ds4}}\right)}$

Output Resistance $r_{out} = r_{ds6}$

Advantages:

1. It has high output voltage swing.
2. It provides a high voltage gain to the user.
3. Noise associated with this op-amp is quite low.

Disadvantages:

1. It has a compromised frequency response.
2. This topology has high power consumption because of two stages in its design.
3. This has a poor negative Power-Supply Rejection at high frequencies.

This op-amp particularly has applications in telecommunication area. After initial success, it was noted that this suffers from a poor PSRR (Power-Supply rejection Ratio).

3. Telescopic Cascode OTA:

Telescopic architecture is the simplest version of the single stage OTA (Operational Transconductance Amplifier). The gain that can be achieved by a single stage is around 40 dB. Thus, in order to achieve 80 dB or so it is necessary to use a cascade of two stages. However, cascading of two stages brings about two poles one close to the other and this requires compensation network, besides increasing the global complexity, reduces the design flexibility[4]. A cascade with cascode load permits us to achieve high gain without the disadvantage of having two poles one close to each other. Therefore the use of cascode based op-amp is an interesting solution alternative to the two stages.

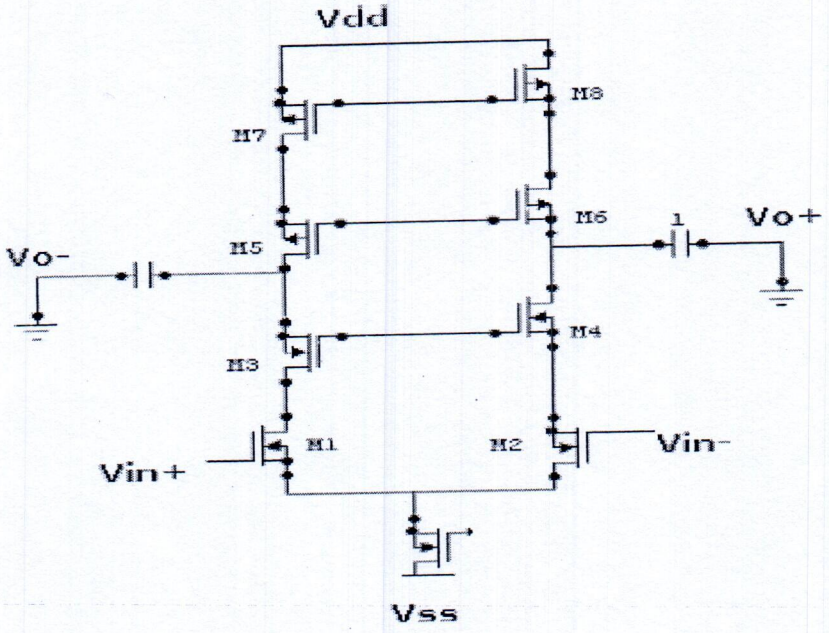


Figure (10) Telescopic amplifier

As shown in architecture (fig. 10), the transistors are placed one on the top of the other to create a sort of Telescopic composition (this led to the circuit name as telescopic ota). The input differential pair injects the signal currents into common gate stages. Then, the circuit achieves the differential to single ended conversion with a PMOS cascode current mirror. In this implementation limiting the maximum value and "wasting" one PMOS threshold voltage in the swing. First, it provides only half the output voltage swing. Second, it contains a mirror pole at node X, thus limiting the performance of amplifier. The telescopic operational amplifier has smaller swing, which means reduced dynamic range, this is offset somewhat by the lower noise factor. The above reason implies that the Telescopic op-amp is a better candidate for low power, low noise single stage operational transconductance amplifier. The single stage architecture normally suggests low power consumption.

Advantages:

1. The telescopic cascode achieves a gain similar to the one of the two stages architecture, without having two poles one close to each other.

2. Its lower noise factor makes it a better candidate for low power, low noise single stage operational transconductance amplifier. A telescopic cascode op-amp typically has a higher frequency capability and consumes less power than other topologies.

Disadvantages:

1. Telescopic op-amp has severely limited output swing and hence the dynamic range. It is smaller than that of Folded Cascode because the tail transistor directly cuts into output swing from both side of op-amp.
2. Another drawback of telescopic cascode is the difficulty in shorting their inputs and outputs, e.g., to implement a unity gain buffer.

While a cascode is rarely used as a unity gain buffer, some other topologies such as the switched-capacitor circuits require that the input and output of the op amp be shorted for part of the operation period. It is quiet difficult to obtain these specifications.

4. Regulated Cascode (Gain Boosting) OTA

The architecture shown in fig. 11, is commonly called as Regulated Cascode (Gain Boosting) OTA. The cascode is a two-stage amplifier composed of a transconductance amplifier followed by a current buffer.Compared to a single amplifier stage, this combination may have one or more of the following characteristics: higher input-output isolation, higher input impedance, high output impedance, higher gain or higher bandwidth. In modern circuits, the cascode is often constructed from two transistors (BJTs or FETs), with one operating as a common emitter or common source and the other as a common base or common gate. The cascode improves input-output isolation (or reverse transmission) as there is no direct coupling from the output to input. This eliminates the Miller effect and thus contributes to a much higher bandwidth.

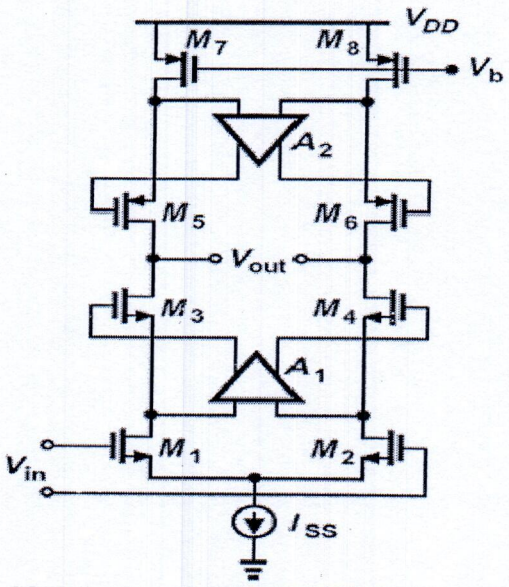


Figure (11) Regulated Cascode OTA

5. Folded Cascode OTA

The architecture shown in fig. 12, is commonly called as Folded Cascode ota. The folded cascode ota was developed to improve the input common mode range and the power-supply rejection ratio performance of the two-stage op-amp. This amplifier is an example of a self-compensated op-amp. It is cascade of a differential transconductance stage with a current stage followed by a cascode current- mirror load. One of the advantages of folded cascode op-amp is that it has a push-pull output. That is, the op-amp can actively sink or source current from load. The output stage of previous two-stage op-amp is class A, which means that either it's sinking or sourcing capability is fixed.

Now important difference between folded cascode and telescopic op-amp circuits are discussed one bias current, Iss, provides the drain current of both the input transistors and cascode devices, It is therefore possible to design the latter to allow shorting its input and output terminal with negligible swing limitation.

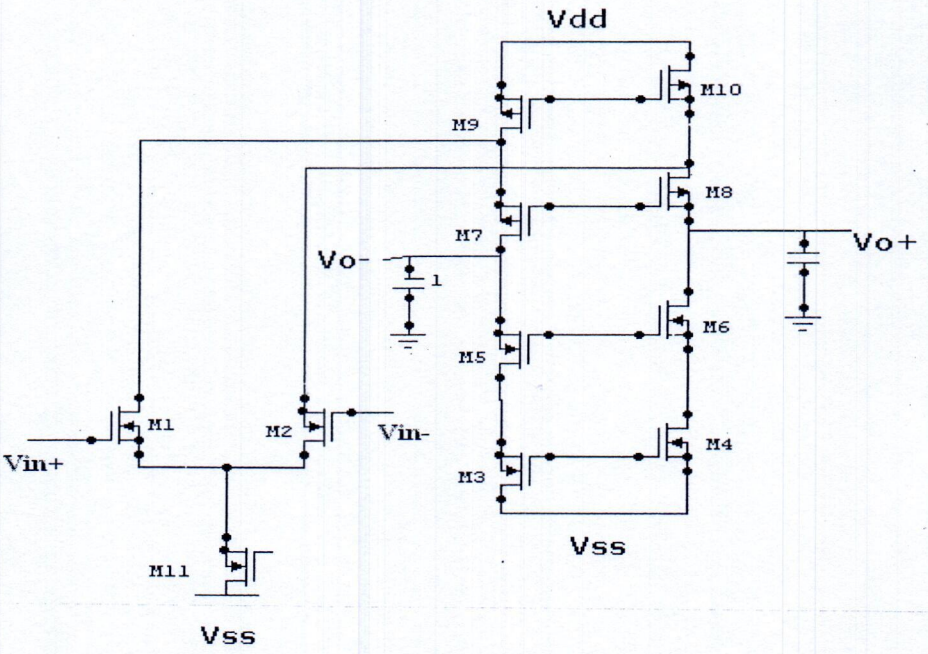


Figure (12) Folded Cascode op-amp

Maximum output swing of the folded cascode op-amp (fig.12) can be calculated by the proper choice of Vb1 and Vb2 . The lower end of the swing is given by $V_{OD3} + V_{OD5}$ and the upper end by $V_{DD} - (|V_{OD7}| + |V_{OD9}|)$. Thus, the peak to peak swing on each side is equal to $V_{DD} - (V_{OD3} + V_{OD5} + |V_{OD7}| + |V_{OD9}|)$.

The folded cascode ota contain PMOS input differential pair exhibits a lower transconductance than does an NMOS pair. Furthermore, r_{01} and r_{05} appear in parallel, reducing the output impedance, especially because M5 carries the current of both the input devices and cascode branch. As a consequence the gain is usually two to three times lower than that of a comparable telescopic cascode.

A folded cascode op amp may incorporate NMOS input devices and PMOS cascode transistors. Such a circuit potentially provides a higher gain than the op amp of fig. 11 because of the greater mobility of NMOS devices, but at the cost of lowering the pole at folding point. This is because pole at node X is given by the product of $1/(g_{m3} + g_{mb3})$ and the total capacitance at this node. The magnitude of both of these components is relatively high: M3 suffers from a low

transconductance and M5 contributes substantial capacitance because it must be wide enough to carry the drain currents of both M1 and M3.

The overall voltage swing of a folded cascode ota is only slightly higher than that of a telescopic configuration. This advantage comes at the cost of higher power dissipation, lower voltage gain, and lower pole frequencies. Folded cascode ota is used quiet widely, even more than telescopic topologies, because the inputs and outputs can be shorted together and choice of common mode level is easier. In a telescopic op amp three voltages must be defined carefully: the input CM level and the gate bias voltages of the PMOS and NMOS cascode transistors, where as in folded-cascode configuration only the latter two are critical.

Chapter – 2

RESEARCH PLAN

Designing high performance analog circuits is becoming increasingly challenging with the persistent trend toward reduced supply voltages. At large supply voltages, there is a trade-off among speed, power and gain, amongst other performance parameters. Often these parameters present contradictory choices for the ota architectures.

The operational transconductance amplifier is probably the most widely used building block in analog IC's. The choice of OTA topologies depends upon the specific application. Comparative analysis of single stage, two stage, folded cascode and telescopic op amps is discussed as per their performance. For high gain and low power application two stage ota are preferred to use. To get faster speed telescopic ota is used and for unity gain buffer folded cascode ota is used.

In many analog applications, operational transconductance amplifier circuitry requires large gain which can be achieved by increasing the number of stages. In addition to high gain, system should maintain its stability. So, in order to improve stability, various compensation techniques are used which incorporates feed forward network or compensating capacitor in multistage amplifier circuit. The position of capacitor depends on input terminal i.e. inverting or non-inverting, of cascading stages. Thus, with the implementation of these techniques, a practical low power, high gain, stable operational transconductance amplifier can be achieved.

2.1 Research Plan:

The existing and new proposed OTAs are explained in the first paper. The conventional 3-OTA based inductor [3] is shown in the Fig. 3. This circuit was implemented using OTA CA3280 which was constructed on transistor level. The proposed 3-OTA based inductor is shown in the Fig. 4. A floating inductor using 3-OTAs with one grounded capacitor has been proposed in the first paper. The work has been focused on 0.5 μm CMOS technology. The inductance can be adjusted with external bias current of OTAs. The proposed circuit has been found to provide a sufficient accuracy and also promisingly applicable to the RLC low pass filter.

Different techniques are proposed [24]–[27] and discussed for decreasing transconductance. Current division technique is uses for implementation of very large time constant. Using this

technique we design a low transconductance OTA which can be used in low frequency application.

After the study about OTA, there is better chance to improve the performance of OTA in terms of: Gain, Phase Margin, CMRR, Slew Rate, PSRR, and Power Dissipation.

And also there is a scope for the design and implementation on the applications of OTA such as: Filters, Converters, Multiplier, etc.

2.2 Goals and Objective:

The objective is to focus on the design of a CMOS OTA to improve the performance. Also the applications like Filter, Multiplier, Converters, etc. based on OTA will be further designed and implemented.

The following goals are aimed to be achieved:

Low Voltage

High Speed

Increased chip density

Less power consumption

Low cost

REFERENCES

[1] Radwene LAAJIMI, "A novel Design of low power and wide bandwidth Operational Transconductance Amplifier Using 0.35µm Technology", Electronics, Micro-technology and Communication (EMC) research group National School of Engineers, Sfax (ENIS), BP W, 3038 Sfax, Tunisia, 978-1-4673-5549-0/13/$31.00 ©2013 IEEE

[2] Soroush Moallemi, Abumoslem Jannesari A New Architecture For Two-Stage OTA with No-Miller Capacitor Compensation, ECE Department, Tarbiat-Modares University Integrated Circuit design Lab Tehran, Iran, 978-1-4673-3119-7/12/$31.00 ©2012 IEEE

[3] Riewruja, V., "Simple square-rooting circuit using OTAs", Electron. Lett., 2008, Vol. 44 No.17, pp. 1000-1002.

[4] Petchmaneelumka W, "Simple floating inductance simulators using OTAs", IEEE I2MTC '09., pp 1018-1021, May 2009.

[5] Koomagaew C, Petchmaneelumka W, Riewruja V,"OTA based Floating Inductance Simulator",ICCAS-SICE, pp 857-860, Aug.. 2009.

[6] Kumngem M, Somdunyakanok M, Prommee P, "High-Input Impedance Voltage-Mode Multifunction Filter with Three-Input Single-Output Based on Simple CMOS OTAs" , ISCIT, pp 426-431, 2009.

[7] Pal, K.: "New inductance and capacitor floatation schemes using current conveyors", Electron. Lett., 1981, vol. 17, no. 21, pp. 807-808.

[8] Singh, V.: "Active RC single-resistance-controlled lossless floating inductance simulation using single grounded capacitor", Electron. Lett., 1981, vol. 17, no. 24, pp 920 -921.

[9] Phillip E. Allen, Douglas R. Holberg, "CMOS Analog circuit Design," 2nd Edition, 2004.

[10] Leung, K.N., Mok, P.K.T., "Analysis of Multistage Amplifier-Frequency Compensation, "IEEE Transactions on Circuits and Systems I, Fundamental Theory and Applications, vol. 48, no. 9, Sep 2001.

[11] You, F., Embabi, S.H.K., Sanchez-Sinencio, E., "Multistage Amplifier Topologies with Nested gm-C Compensation," IEEE Journal of Solid State Circuits, vol.32, no.12, Dec 1997.

[12] Behzad Razavi, "Design of Analog CMOS Integrated circuits," 2nd Edition, 2002.

[13] Mita, R., Palumbo, G., Penissi, S., "Design Guidelines for Reversed Nested Miller Compensation in Three-Stage Ampifiers," IEEE Transaction on Circuits and Systems II, Analog and Digital Signal Processing, vol.50, no.5, pp. 227-233, May 2003.

[14] Zhu, F., Yan, S., Hu, J., Sanchez-Sinencio, E., "Feedforward Reversed Nested Miller Compensation Techniques for Three-Stage Amplifiers," IEEE International Symposium on Circuits and Systems, vol.3, pp. 2575-2578, May 2005.

[15] R. Jacob Baker, Harry W. Li, David E. Boyce , "CMOS circuit design, layout and simulation," 2nd edition ,2000.

[16] W. Kiranon and P. Pawarangkoon, "Floating inductance simulation based on current conveyors," *Electron. Lett.*, vol. 33, no. 21, pp. 1748-1749, 1997.

[17] G. Ferri, N.C. Guerrini, and M. Diqual, "CCII-based floating inductance simulator with compensated series resistance," *Electron. Lett.*, vol. 39, no. 22, pp. 1560-1562, 2003.

[18] P.R. Kinget, "Device Mismatch and Tradeoffs in the Design of Analog Circuits", *"IEEE Journal of Solid State Circuits,"* vol. 40, no. 6, pp. 1212-1224, 2005.

[19] WANG Jin and QIU Yulin, "Analysis and Design of Fully Differential Gain-Boosted Telescopic Cascode Op-amp", Institute of Microelectronic of Chinese Academy of Sciences, Beijing, 100029, China, year 2004 IEEE,

[20] Antonio J. López-Martín, "Low-Voltage Super Class AB CMOS OTA Cells With Very High Slew Rate And Power Efficiency", IEEE Journal Of Solid-State Circuits, Vol. 40, No. 5, May 2005

[21] Li Tianwang, Ye Bo, and Jiang Jinguang, "A Novel Fully Differential Telescopic Operational Transconductance Amplifier", Journal of Semiconductors, Vol. 30, No. 8, August 2009

[22] Zahra Haddad Derafshi and Mohammad HosseinZarifi,"Low-Power High-Speed OTA in 0.35μm CMOS Process", European Journal of Scientific Research, ISSN 1450-216X Vol.37 No.3 (2009), pp.368-375

[23] D. Nageshwarrao, S.VenkataChalamand ,V.MalleswaraRao, "Gain Boosted Telescopic OTA With 110db Gain And 1.8GHz. UGF", International Journal of Electronic Engineering Research, ISSN 0975 - 6450 Volume 2 Number 2 (2010) pp. 159 -16

[24] CarstenWulff, TrondYtterdal, "High Speed, High Gain OTA in a Digital 90nmCMOS Technology", Department of Electronics and Telecommunication, Norwegian University of Science and Technology, N- 7491 Trondheim, Norway